

to determine/calculate the peak current and average rectified current for each processor half cycle. Peak current is the highest current measured for a given processor half cycle (i.e., the highest detected current value for any given measurement period within the processor half cycle). Average rectified current is the average of the rectified current measurements over the processor half cycle (i.e., the average of the rectified current measured for each of the measurement periods constituting the processor half cycle; e.g., 32).

[0150] For each measurement period the processor **100** also analyzes the frequency of the signal to determine if low frequency or high frequency signals/noise are detected. Based on the frequency detected, one or more counters may be incremented/decremented, or adjusted. Alternately, the detected frequencies may be recorded/stored in any suitable manner. In at least one embodiment, if processor **100** determines that the frequency measured/sensed for a given measurement period is within a certain predetermined low frequency range, e.g., $2 < 4$ MHz, a counter Nlo is incremented. If processor **100** determines that the frequency measured/sensed for a given measurement period is within a certain predetermined high frequency range, e.g., 4-10 MHz, a counter Nhi is incremented. Alternatively, processor **100** could be programmed to increment the high frequency counter Nhi if it determines that the measured/sensed frequency is greater than a certain predetermined value; e.g., 4 MHz.

[0151] For each processor half cycle, processor **100** carries out a set of instructions to monitor the data being collected, computed and/or stored to determine if certain conditions, or events, have occurred. In particular, processor **100** monitors for voltage drop values and current peaks that meet or exceed certain predetermined values. If the processor determines that a voltage drop between any two consecutive processor half cycles is greater than a certain predetermined value, e.g., any one of 25-100 volts or more particularly 50-60 volts or even more particularly 50 volts, 55 volts or even 60 volts, then the processor sets a voltage drop flag (VDF) associated with the processor half cycle under consideration. Alternatively, voltage drop flag VDF may be implemented via a counter, or any other suitable memory element. If the processor detects both that: a peak current value for the processor half cycle under consideration meets or exceeds a certain predetermined value/threshold, e.g., 24 amps or for example any one of a range of values such as but not limited to 5 amps, 20 amps, 100 amps or, for example any one of a range of values 5-100 amps; and there was either, or both, low or/and high frequency noise detected during the processor half cycle, then the processor would increment a parallel arc interval counter (PC). The processor then determines if this was the first parallel arc pulse/signal detected (e.g., $PC=1$). If this was the first parallel arc pulse, then the processor would initialize a parallel arc timer for a period of one half second (0.5 sec). The processor would then continue to update the parallel arc interval counter PC for the remaining duration of the parallel arc timer period, incrementing the counter if the prescribed conditions are met for any subsequent processor half cycles within the parallel arc timer period. During this parallel arc timer period, the processor also maintains/updates a current rise/jump counter (IRC) and a current break/drop counter (IBC).

[0152] The current rise/jump counter is incremented by the processor when it determines that the difference in the

measured rectified current between two successive measurement periods within the processor half cycle is greater than a certain predetermined value; e.g., a difference of 20 amps measured between any two successive measurement periods. While an example of 20 amps is provided above, other values could be used such as but not limited to 5 amps, 10 amps, 25 amps or any one of a range such as 5-100 amps.

[0153] The current break counter is incremented by the processor when it determines that for the processor half cycle under consideration: the parallel arc interval counter is non-zero and either: (a) the average rectified current is below a predetermined value (e.g., any one of but not limited to: 6 amps, 5 amps, 1 amps, 10 amps 20 amps, 100 amps or an one of a range of values between 1-100 amps), or (b) the peak current is below a predetermined value (e.g., 10 amps or any one of but not limited to: 6 amps, 5 amps, 1 amps, 20 amps, 100 amps or an one of a range of values between 1-100 amps).

[0154] In addition to the peak current being determined/evaluated by the processor for each processor half cycle, two peak current counters are employed by the processor during the parallel arc timer period to track peak currents that are greater than certain predetermined values. In at least one embodiment, there are two peak current counters denoted as Nbig and Nhuge. Peak current counter Nbig is incremented when the peak current for a processor half cycle within the parallel arc timer period is greater than a first threshold; e.g., 65 amps or any one of but not limited to: 30 amps, 50 amps, 70 amps, or 100 amps or any one of a range of values between 1-100 amps. Peak current counter Nhuge is incremented when the peak current for a processor half cycle within the parallel arc timer period is greater than a second threshold; e.g., 100 amps or any one of but not limited to: 30 amps, 50 amps, 70 amps, or 110 amps, 200 amps or any one of a range of values between 1-200 amps. Processor **100** may also be programmed with a set of instructions to maintain/update a noise counter NC during the parallel arc timer period which is incremented by processor **100** if it determines that during the parallel arc timer period any given processor half cycle is evaluated to be an arcing half cycle (i.e., the arcing array/shift register value for that processor half cycle equals "1").

[0155] With reference to FIG. 4C and the previously described counters, variables, flags, values and arcing array, a process carried out by the processor for determining whether a dangerous parallel arcing condition exists or has occurred will now be described. In at least one preferred embodiment, processor **100** evaluates a number of conditions/criteria to determine whether a dangerous parallel arc fault condition has occurred or exists and whether or not the device should then signal the interrupting mechanism to interrupt one or more of the conductive paths as well as possibly indicate such condition as discussed above.

[0156] For example, as shown in FIG. 4C, in step S20, processor **100** determines whether a peak current for any given processor half cycle is greater than a predetermined level. In at least one example, this predetermined level is 24 Amps but as discussed above, this value could be different or selected from a range provided above. In step S21 processor **100** detects whether there is a signal with a frequency indicative of noise on the line (i.e., one or both of the counters Nhi or Nlo has a value greater than "1"). If both conditions (peak current above a predetermined level and noise is present) are true, in step S22, processor **100** incre-